REMARKS

This Amendment is responsive to the Office Action dated April 20, 2005. All objections and rejections of the Examiner are respectfully traversed. Reconsideration and further examination is respectfully requested.

In paragraphs 3-26 of the Office Action the Examiner rejected claims 1-33 under 35 U.S.C. 102(b), citing United States patent number 4,817,080 of Soha ("Soha"). Applicants respectfully traverse these rejections.

Soha discloses a monitoring system for a local-area network in which a monitor manager system receives information from monitor units connected to the local-area network. The monitor units of Soha employ counters in a packet memory that are dynamically allocated to specific packet characteristics as new packet characteristics appear on the network. A look-up table associates the Soha counters with the corresponding characteristics, and a look-up engine operates the look-up table to search for the location of specific counters by employing a binary-search method to perform processing for a packet within the minimum packet time.

The monitor unit of Soha places the contents of a received packet into successive packet-memory locations. Interfaces to the Soha monitor unit place packet size and the locations of stored received packet contents into the packet memory. The Soha interface then interrupts a microprocessor, which operates from a program stored in its program memory to update counters, consisting of packet-memory locations, that maintain statistics.

In Figs. 5 and 6 of Soha, the blocks on the left-hand side represent input information from the packet-buffer section of memory, while the blocks on the right-hand side represent the

resultant updating of counters. As shown in Fig. 5 of Soha, a block 60 represents operation of a packet counter. As stated in Soha at column 6 in lines 55 - 69, the microprocessor operates in response to an interrupt by "by fetching the contents of a predetermined location in the packet memory 50 that serves as a packet counter, incrementing those contents, and writing them back into that location Level 58 contains only block 60, on the right side of the drawing to represent the operation on the packet counter; it has no block on the left side. ***This indicates that the microprocessor does not need to know anything about the packet in order to perform this function; it needs only to know that a packet was received, and its interruption by local-area-network interface 46 or 48 represents this fact***" (emphasis added). Accordingly, Soha expressly teaches independently updating a separate packet counter 58 (106 in Fig. 6) prior to any further processing of the received packet, such as determining a byte count of the received packet, and/or updating a byte counter.

This is further shown by the separate second level 62 of Fig. 5 in Soha, which illustrates a subsequent operation, performed after writing the packet count as described above, in which the microprocessor fetches a count of the number of bytes in the received packet, and then updates a packet memory location serving as a counter for the total number of bytes that have been transmitted on the local-area network. As stated in column 7 lines 10-14, the Soha system operates such that the "microprocessor fetches the contents of that location, adds to them the packet byte count that it fetched from the packet-storage part of the packet memory 50, and returns the results to that location." The fact that the packet and byte counters of Soha are stored in two separate memory locations is further emphasized at line 15 of column 7, which states:

> In both of the ***operations*** represented by levels 58 and 62, the location of the counter to be updated was predetermined; the program memory 53 contains the ***locations*** of the ***packet and byte counters***, so the microprocessor does not have to employ the look-up engine 54 and the look-up table 56 in order to locate the counter of interest. (emphasis added)

Thus it is clear that the packet and byte counters of Soha consist of separate memory locations that are updated and stored in separate, independent operations upon receipt of a packet.

Nowhere in Soha is there disclosed or suggested any system or method for monitoring a network including:

> receiving at least one data packet;
> reading an entry of a memory device, ***the entry of the memory device containing both a first statistical value and a second statistical value, wherein the entry is a single memory location of the memory device, wherein the first statistical value includes a packet count, and wherein the second statistical value includes a byte count***;
> determining a third statistical value based on at least one of a content of the at least one data packet, the first statistical value, and the second statistical value; and
> storing the determined third statistical value in the entry of the memory device. (emphasis added)

as in the present independent claim 1. Independent claims 12 and 23 include analogous features. In contrast, Soha describes a system in which packet and byte counters are stored in separate memory locations that are updated in separate, independent operations. In further contrast, the lookup table memory 56 of Fig. 4 in Soha is made up of 64 bit memory locations, each storing a tag portion 75 corresponding to a portion of a source address in a received packet, as well as a pointer portion 76. As stated beginning at line 53 of column 7 in Soha:

> . . . the look-up engine 54 searches the locations for one whose tag segment ***contains the source-address code*** that the microprocessor 52 supplied to the look-up engine 54. If it finds such a location, it sends microprocessor 52 the contents of the ***pointer segment*** of that location, and the microprocessor 52 increments the contents of the location ***whose address the pointer represents***. (emphasis added)

Thus Soha teaches a system in which tag fields may be combined with pointers in 64-bit memory locations, but in which byte and packet counters are stored in *separate, independently maintained memory locations*. This stands in clear opposition to the present independent claims, in which an entry of the memory device contains both a first statistical value and a second statistical value, wherein the entry is a single memory location of the memory device, wherein the first statistical value includes a packet count, and wherein the second statistical value includes a byte count.

For the above reasons, Applicants respectfully urge that Soha does not disclose or suggest all the features of the present independent claims 1, 12 and 23. Accordingly, Soha does not anticipate the present independent claims 1, 12 and 23 under 35 U.S.C. 102. As the remaining claims depend either directly or indirectly from claims 1, 12, and 23, they are respectfully believed to be patentable over Soha for at least the same reasons.

In paragraphs 27-33 of the Office Action, the Examiner rejected claims 34-39 as being obvious under 35 U.S.C. 103, citing Soha in combination with United States patent number 6,687,247 of Wilford et al. ("Wilford et al.") Applicants respectfully traverse these rejections.

Nowhere in the combination of Soha and Wilford et al. is there disclosed or suggested any system or method for monitoring a network, that includes:

> receiving at least one data packet;
> reading an entry of a memory device, ***the entry of the memory device containing both a first statistical value and a second statistical value, wherein the entry is a single memory location of the memory device, wherein the first statistical value includes a packet count, and wherein the second statistical value includes a byte count;***

determining a third statistical value based on at least one of a content of the at least one data packet, the first statistical value, and the second statistical value; and

storing the determined third statistical value in the entry of the memory device. (emphasis added)

as in the present independent claims 1, 12 and 23, from which claims 34-39 depend. Applicants first respectfully urge that there is not sufficient motivation to combine Soha and Wilford et al. A *prima facie* case of obviousness under 35 U.S.C. 103 must include a showing of a suggestion, teaching or motivation that would have led a person of ordinary skill in the art to combine the cited references *in the particular manner claimed.* See In re Dembiczak, 175 F.3d 994, 998 (Fed. Cir. 1999), and In re Kotzab, 217 F.3d 1365, 1371 (Fed. Cir. 2000). In the present case, the combination of Soha and Wilford et al. provides no hint or suggestion of even the desirability of providing any system or method that includes *storing both a packet count and byte count in a single memory location*, as in the present independent claims 1, 12 and 23, from which claims 34-39 depend. Applicants further respectfully urge that Soha teaches away from providing packet and byte counts in a single memory location by its teaching of the levels 58 and 62 of Fig. 5, which explicitly include separate steps for incrementing packet and byte counters, in which the packet count is incremented before any other information is determined about the received packet. Thus a person skilled in the art would not be motivated to modify Soha in the manner of the present independent claims 1, 12 and 23, from which claims 34-39 depend, since such modification would destroy the independence of the steps provided by the levels 58 and 62 in Fig. 5 of Soha.

Even if a sufficient motivation were present to combine Soha and Wilford et al. in the manner of the present claims, and Applicants make no admission that such motivation exists, the combination of Soha and Wilford et al. still does not teach the present claims 1, 12 and 23, from

which claims 34-39 depend. As discussed above with regard to the rejections under 35 U.S.C. 102, Soha teaches a system in which tag fields may be combined with pointers, but in which byte and packet counters are expressly described as stored in separate, independently maintained memory locations. As noted in Applicants' previous response, beginning at line 43 of column 52 Wilford et al., describe a Committed Access Rate (CAR) Statistics Module beginning that receives data from the Token Bucket Module in Fig. 30. With regard to counters, Wilford et al. state as follows:

> The CAR Statistics Module keeps a count of all packets and bytes passed and dropped per token bucket. The packet ***counters*** are 32 bits and byte ***counters*** 40 bits. The drop ***counters*** will be approximately 4 bits smaller as we should not be dropping at full line rate for very long so packet drop ***counters*** are 28 bits and byte drop counters are 36 bits. All of these ***counters*** should saturate (i.e. not roll over) and clear when read by the CPU.

Wilford et al. provide no other discussion of counters. Accordingly, the teaching of Wilford et al. regarding packet count and byte count statistics is limited to providing counters of some kind, without a hint or suggestion as to the specific structure or operation of the counters, beyond suggested sizes, and that the counters should not roll over. Like Soha, Wilford et al. lacks any teaching that would lead one skilled in the art to the present independent claims in which ***a single memory location of a memory device is used to store both a packet count and a statistical value including a byte count.*** The mere teaching of a "counter" of some kind in Wilford et al., combined with Soha's disclosure of separately located and independently maintained packet and byte counters, fails to describe or suggest any system or method having an entry of the memory device containing both a first statistical value and a second statistical value, wherein the entry is a single memory location of the memory device, wherein the first statistical value includes a packet

count, and wherein the second statistical value includes a byte count, as in the present independent claims.

For the above reasons, Applicants respectfully urge that the combination of Soha and Wilford et al. fails to disclose or suggest all the features of the present independent claims 1, 12 and 23, from which claims 34-39 depend. Accordingly, the combination of Soha and Wilford et al. does not support a *prima facie* case of obviousness with regard to the present independent claims 1, 12 and 23 under 35 U.S.C. 103. As to claims 34-39, they each depend either directly or indirectly from independent claims 1, 12 and 23, and are respectfully believed to be patentable over the combination of Soha and Wilford et al. for at least the same reasons. Reconsideration of all pending claims is respectfully requested.

In view of the above, Applicants respectfully urge that the present claims are allowable, and respectfully request that all rejections of the Office Action be withdrawn.

Applicants have made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone David A. Dagg, Applicants' Attorney at 617-630-1131 so that such issues may be resolved as expeditiously as possible.

For these reasons, and in view of the above amendments, this application is now considered to be in condition for allowance and such action is earnestly solicited.

Respectfully Submitted,

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Date

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